IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of

Applicants	:	John D. Porter and William N. Thompson
Serial No.	:	09/~~750,174~~ 740 174
Filed	:	December 18, 2000
Title	:	LATCH-UP PREVENTION FOR MEMORY CELLS
Docket No.	:	MIO 0042 V2

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on March 22, 2001.

Gregory J. Adams 44,494
Reg. No.

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

SECOND PRELIMINARY AMENDMENT

Please disregard the preliminary amendment filed on December 18, 2000. Or, in the alternative, cancel claims 78-81 added in the first preliminary amendment filed on December 18, 2000. The preliminary amendment filed on December 18, 2000, contained an error in claim numbering.

IN THE SPECIFICATION

At page 1 after the Title, please insert the following:

--CROSS REFERENCE TO RELATED APPLICATIONS

This application is a divisional of U.S. Patent Application Serial No. 09/368,710, filed August 5, 1999, which is itself a divisional of U.S. Patent Application Serial No. 09/045,465, filed March 20, 1998, and issued as a patent, U.S. Patent No. 6,005,797, on December 21, 1999.--

IN THE CLAIMS

Please cancel claims 1-40 in the application.

Please note that the claims in the as-filed application were misnumbered in that claims 21-30 were missing. Claims 21-30 have been canceled to avoid any confusion.

Please add the following claims:

Please add the following new claims:

41. A method of fabricating a memory cell comprising:

providing a substrate comprising a semiconductor layer;

forming a first inverter in the semiconductor layer;

forming a second inverter in the semiconductor layer;

forming a first parasitic resistance in the semiconductor layer and coupling the first parasitic resistance to the first inverter;

forming a second parasitic resistance in the semiconductor layer and coupling the second parasitic resistance to the second inverter; and

cross-coupling the second inverter to the first inverter.

42. The method of claim 41, wherein forming a first inverter comprises:

forming a source, drain and gate of a first transistor in the semiconductor layer;

coupling the source of the first transistor to the first parasitic resistance;

forming a first node;

coupling the drain of the first transistor to the first node;

forming a source, drain and gate of a second transistor in the semiconductor layer; and

coupling the drain of the second transistor to the first node.

43. The method of claim 42, wherein forming a second inverter comprises:

forming a source, drain and gate of a third transistor in the semiconductor layer;

forming a second node;

coupling the source of the third transistor to the second parasitic resistance;

coupling the drain of the third transistor to the second node;

forming a source, drain and gate of a fourth transistor in the semiconductor layer; and

coupling the drain of the fourth transistor to the second node.

44. The method of claim 43, wherein cross-coupling the second inverter to the first inverter comprises:

coupling the gate of the first transistor to the second node;

coupling the gate of the second transistor to the second node;

coupling the gate of the third transistor to the first node; and

coupling the gate of the fourth transistor to the first node.

45. A method of fabricating a first inverter comprising:

providing a semiconductor;

doping the semiconductor to provide a first type conductivity;

forming a well in the semiconductor having a second type conductivity;

forming a first type transistor in the well;

forming a second type transistor in the substrate outside of the well;

forming a first contact in the well; and

forming a second contact in the well, wherein the second contact is separated from the first contact by the first type transistor.

46. The method of claim 45, wherein forming a first contact comprises forming a first contact a first distance from the second type transistor, wherein the first distance determines a first resistance and wherein forming a second contact comprises forming a second contact a second distance from the second type transistor, wherein the second distance determines a second resistance.

47. The method of claim 45, wherein forming a well comprises forming an n-type well in the semiconductor, wherein forming a first type transistor comprises forming a first p-

type region in the well for a source, forming a second p-type region in the well for a drain and forming a gate over the well, and wherein forming a second type transistor comprises forming a first n-type region in the substrate for a source, forming a second n-type region in the substrate for a drain and forming a gate over the substrate.

48. A method for fabricating a memory cell comprising:

providing a semiconductor;

doping the semiconductor to provide p-type conductivity;

forming a first inverter, wherein forming a first inverter comprises:

forming a well in the semiconductor having a n-type conductivity;

forming a p-type transistor in the well;

forming a n-type transistor in the substrate outside of the well;

forming a first contact in the well; and

forming a second contact in the well, wherein the second contact is separated from the first contact by the second type transistor;

forming a second inverter, wherein forming a second inverter comprises:

forming a well in the semiconductor having a n-type conductivity;

forming a p-type transistor in the well;

forming a n-type transistor in the substrate outside of the well;

forming a first contact in the well; and

forming a second contact in the well, wherein the second contact is separated from the first contact by the second type transistor; and

cross coupling the second inverter to the first inverter.

49. A method of fabricating a semiconductor device comprising:

providing a semiconductor;

forming a source and drain in the semiconductor;

determining a desired parasitic resistance;

calculating a desired distance; and

forming a contact over the semiconductor by the desired distance from the source to create the desired resistance between the contact and the source.

50. A method of fabricating a semiconductor device comprising:

providing a semiconductor;

forming a source of a transistor in the semiconductor;

determining a desired parasitic resistance;

calculating a first desired distance and a second desired distance according to a first resistance and a second resistance;

forming a first contact over the semiconductor by the first desired distance from the source creating the first resistance;

forming a second contact over the semiconductor by the second desired distance from the source opposite the first contact creating the second resistance; and

wherein the desired parasitic resistance is equal to the sum for the first resistance and the second resistance.

51. A method of fabricating a memory cell comprising:

providing a semiconductor;

forming a first semiconductor structure in the semiconductor;

forming a first parasitic resistor in the semiconductor;

forming a second semiconductor structure in the semiconductor;

forming a second parasitic resistor in the semiconductor;

electrically coupling the first parasitic resistor to the first semiconductor structure;

electrically coupling the second parasitic resistor to the second semiconductor structure; and

electrically coupling the first semiconductor structure to the second semiconductor structure.

52. A method of fabricating a memory cell comprising:

providing a substrate;

forming a first semiconductor structure within the substrate;

forming a first pull-up transistor within the first semiconductor structure by forming a first source and a first drain in the substrate and forming a first gate over the substrate;

forming a first pull-down transistor within the first semiconductor structure by forming a second source and a second drain in the substrate and forming a second gate over the substrate;

forming a first contact and a second contact within the first semiconductor structure;

coupling the first drain to the second drain;

coupling the first gate to the second gate; and

coupling the first source to the second contact and coupling the first contact to a first voltage input such that the first source is coupled to the first voltage input through parasitic resistance of the first semiconductor structure.

53. A method of fabricating a memory cell comprising:

providing a substrate;

forming a first semiconductor structure and a second semiconductor structure within the substrate;

forming a first pull-up transistor within the first semiconductor structure by forming a first source and a first drain in the substrate and forming a first gate over the substrate;

forming a first pull-down transistor within the first semiconductor structure by forming a second source and a second drain in the substrate and forming a second gate over the substrate;

forming a first contact and a second contact within the first semiconductor structure;

forming a second pull-up transistor within the second semiconductor structure by forming a third source and a third drain in the substrate and forming a third gate over the substrate;

forming a second pull-down transistor within the first semiconductor structure by forming a fourth source and a fourth drain in the substrate and forming a fourth gate over the substrate;

forming a third contact and a fourth contact within the second semiconductor structure;

coupling the first drain to the second drain and the third drain to the fourth drain;

coupling the first gate to the second gate and the third gate to the fourth gate;

coupling the first source to the second contact and coupling the first contact to a first voltage input such that the first source is coupled to the first voltage input through parasitic resistance of the first semiconductor structure; and

coupling the third source to the fourth contact and coupling the third contact to the first voltage input such that the first source is coupled to the first voltage input through parasitic resistance of the second semiconductor structure.

54. The method of claim 53, further comprising:

doping the substrate to form a p-type conductivity; and

forming a n-type well within the first semiconductor structure.

55. The method of claim 54, further comprising forming a n-type well within the second semiconductor structure.

56. A method of fabricating an SRAM memory array comprising:

providing a substrate;

forming a plurality of memory cells arranged in rows and columns, each of the plurality of memory cells fabricated by:

forming a first semiconductor structure within the substrate;

forming a second semiconductor structure within the substrate;

forming a first pull-up transistor within the first semiconductor structure by forming a first source and a first drain in the substrate and forming a first gate over the substrate;

forming a first pull-down transistor within the first semiconductor structure by forming a second source and a second drain in the substrate and forming a second gate over the substrate;

forming a first contact and a second contact within the first semiconductor structure;

forming a second pull-up transistor within the second semiconductor structure by forming a third source and a third drain in the substrate and forming a third gate over the substrate;

forming a second pull-down transistor within the first semiconductor structure by forming a fourth source and a fourth drain in the substrate and forming a fourth gate over the substrate;

forming a third contact and a fourth contact within the second semiconductor structure;

forming a first terminal and a second terminal of a first access transistor in the substrate;

forming a third terminal and a fourth terminal of a second access transistor in the substrate

coupling the first drain to the second drain and the third drain to the fourth drain;

coupling the first gate to the second gate and the third gate to the fourth gate;

coupling the first terminal to the first and second drains;

coupling the third terminal to the third and fourth drains;

coupling the first source to the second contact and coupling the first contact to a first voltage input such that the first source is coupled to the first voltage input through parasitic resistance of the first semiconductor structure; and

coupling the third source to the fourth contact and coupling the third contact to the first voltage input such that the first source is coupled to the first voltage input through parasitic resistance of the second semiconductor structure;

coupling the first and second access gates of each of the plurality of memory cells to respective row lines;

coupling the second terminals of each of the plurality of memory cells to respective first column lines; and

coupling the fourth terminals of each of the plurality of memory cells to respective second column lines.

57. A method of fabricating a memory device comprising:

forming a first semiconductor structure;

forming a first pull-up transistor within the first semiconductor structure by forming a first source, a first drain and a first gate;

forming a first pull-down transistor within the first semiconductor structure by forming a second source, a second drain, and a second gate;

forming a first contact and a second contact within the first semiconductor structure;

coupling the first drain to the second drain;

coupling the first gate to the second gate; and

coupling the first source to the second contact and coupling the first contact to a first voltage input such that the first source is coupled to the first voltage input through parasitic resistance of the first semiconductor structure.

58. A method of fabricating a memory device:

forming a first semiconductor structure and a second semiconductor structure;

forming a first pull-up transistor within the first semiconductor structure by forming a first source, a first drain, and a first gate;

forming a first pull-down transistor within the first semiconductor structure by forming a second source, a second drain, and a second gate;

forming a first contact and a second contact within the first semiconductor structure;

forming a second pull-up transistor within the second semiconductor structure by forming a third source, a third drain, and a third gate;

forming a second pull-down transistor within the first semiconductor structure by forming a fourth source, a fourth drain, and a fourth gate;

forming a third contact and a fourth contact within the second semiconductor structure;

coupling the first drain to the second drain and the third drain to the fourth drain;

coupling the first gate to the second gate and the third gate to the fourth gate;

coupling the first source to the second contact and coupling the first contact to a first voltage input such that the first source is coupled to the first voltage input through parasitic resistance of the first semiconductor structure; and

coupling the third source to the fourth contact and coupling the third contact to the first voltage input such that the first source is coupled to the first voltage input through parasitic resistance of the second semiconductor structure.

59. The method of claim 58, further comprising:

doping the substrate to form a p-type conductivity; and

forming a n-type well within the first semiconductor structure.

60. A method of fabricating a memory device comprising:

forming a plurality of memory cells arranged in rows and columns, each of the plurality of memory cells fabricated by:

forming a first semiconductor structure;

forming a second semiconductor structure;

forming a first pull-up transistor within the first semiconductor structure by forming a first source, a first drain, and a first gate;

forming a first pull-down transistor within the first semiconductor structure by forming a second source, a second drain, and a second gate;

forming a first contact and a second contact within the first semiconductor structure;

forming a second pull-up transistor within the second semiconductor structure by forming a third source, a third drain, and a third gate;

forming a second pull-down transistor within the first semiconductor structure by forming a fourth source, a fourth drain, and a fourth;

forming a third contact and a fourth contact within the second semiconductor structure;

forming a first terminal and a second terminal of a first access transistor in the substrate;

forming a third terminal and a fourth terminal of a second access transistor in the substrate

coupling the first drain to the second drain and the third drain to the fourth drain;

coupling the first gate to the second gate and the third gate to the fourth gate;

coupling the first terminal to the first and second drains;

coupling the third terminal to the third and fourth drains;

coupling the first source to the second contact and coupling the first contact to a first voltage input such that the first source is coupled to the first voltage input through parasitic resistance of the first semiconductor structure; and

coupling the third source to the fourth contact and coupling the third contact to the first voltage input such that the first source is coupled to the first voltage input through parasitic resistance of the second semiconductor structure;

coupling the first and second access gates of each of the plurality of memory cells to respective row lines;

coupling the second terminals of each of the plurality of memory cells to respective first column lines; and

coupling the fourth terminals of each of the plurality of memory cells to respective second column lines.

Docket MIO 0042 V2

REMARKS

Claims 41-56 of the present application were subject to a restriction requirement as claims 62-77 in U.S. Patent Application Serial No. 09/368,710 and were withdrawn from consideration. Claims 57-60 of the present application are new claims and include subject matter not taught by the art of record. Claims 1-40 have been canceled. Thus, claims 41-60 are now pending in the present application.

Applicants respectfully submit that the present application is in condition for allowance. The Examiner is encouraged to contact the undersigned to resolve efficiently any formal matters or to discuss any aspects of the application or of this response. Otherwise, early notification of allowable subject matter is respectfully solicited.

Respectfully submitted,
KILLWORTH, GOTTMAN, HAGAN
& SCHAEFF, L.L.P.

By _____
Gregory J. Adams
Registration No. 44,494

One Dayton Centre
One South Main Street, Suite 500
Dayton, Ohio 45402-2023
Telephone: (937) 223-2050
Facsimile: (937) 223-0724
e-mail: adamsg@kghs.com